Electronics Packaging Forum Multichip Module Technology Issues

Provides coverage on the full range of topics associated with polyimides, including structure, polymer fundamentals, and product areas. The text addresses both basic and applied aspects of the subject. It details the synthesis of polyimides, polyamideimides, and flourinated polyimides, explains the molecular design of photosensitive polyimides, and more.

Foldable Flex and Thinned Silicon Multichip Packaging Technology presents newly emerging methods used to make stacked chip packages in the so-called 2-1/2 D technology (3-D in physical format, but interconnected only through the circuits on folded flex). It is also being used in single chip packages where the thinness of the chips and the flex substrate made packages significantly thinner than through any other means.

Electronics has become the largest industry, surpassing agriCUlture, auto. and heavy metal industries. It has become the industry of choice for a country to prosper, already having given rise to the phenomenal prosperity of Japan. Korea. Singapore. Hong Kong. and Ireland among others. At the current growth rate,

total worldwide semiconductor sales will reach $300B by the year 2000. The key electronic technologies responsible for the growth of the industry include semiconductors. the packaging of semiconductors for systems use in auto, telecom, computer, consumer, aerospace, and medical industries. displays. magnetic, and optical storage as well as software and system technologies. There has been a paradigm shift, however, in these technologies. from mainframe and supercomputer applications at any cost. to consumer applications at approximately one-tenth the cost and size. Personal computers are a good example. going from $500IMIP when products were first introduced in 1981, to a projected $IIMIP within 10 years. Thin. light portable. user friendly and very low-cost are. therefore. the attributes of tomorrow's computing and communications systems. Electronic packaging is defined as interconnection. powering, cool ing, and protecting semiconductor chips for reliable systems. It is a key enabling technology achieving the requirements for reducing the size and cost at the system and product level.

A summary of progress in ball grid array (BGA) packaging technology, for professionals in BGA research and development, and for manufacturers researching BGA for their interconnect systems. Discusses economic, design, material, process, and quality issues, and describes techniques for processing

substrates, routing PCB, assembling CBGA, PBGA, and TBGA packages, and inspection of BGA PCB assemblies. Includes treatment of BGA industry infrastructure, and an electronic packaging glossary. Contains bandw photos and diagrams. Annotation copyright by Book News, Inc., Portland, OR

Important topics covered include building long-term reliability by increasing polyimide stability, recent discoveries in the field of soldering phenomena relating to fundamental fluid mechanical processes, circuit and electromagnetic solutions to problems of modeling highspeed electrical interconnections, how to use the finite-difference time-domain approach in electromagnetic modeling, and the development of dedicated test chips for package evaluation in varied field conditions.

If you design electronics for a living, you need Robust Electronic Design Reference Book. Written by a working engineer, who has put over 115 electronic products into production at Sycor, IBM, and Lexmark, Robust Electronic Design Reference covers all the various aspects of designing and developing electronic devices and systems that: -Work. -Are safe and reliable. -Can be manufactured, tested, repaired, and serviced. -May be sold and used worldwide. -Can be adapted or enhanced to meet new and changing requirements.

A guide to flip chip technologies, for professionals in flip chip and MCM research

and development, and for engineers and technical managers choosing design and manufacturing processes for electronic packaging and interconnect systems. Discusses economic, design, material, quality, and reliability issues of flip chip technologies, and details aspects of classical solder-bumped flip chip interconnect technologies; the next generations of flip chip technologies; and known-good-die testing for multiple module applications. Annotation copyright by Book News, Inc., Portland, OR

This comprehensive book will provide both fundamental andapplied aspects of adhesion pertaining to microelectronics in asingle and easily accessible source. Among the topics to be coveredinclude; Various theories or mechanisms of adhesion Surface (physical or chemical) characterization of materials asit pertains to adhesion Surface cleaning as it pertains to adhesion Ways to improve adhesion Unraveling of interfacial interactions using an array ofpertinent techniques Characterization of interfaces / interphases Polymer-polymer adhesion Metal-polymer adhesion (metallized polymers) Polymer adhesion to various substrates Adhesion of thin films Adhesion of underfills Adhesion of molding compounds Adhesion of different dielectric materials Delamination and reliability issues in packaged devices Interface mechanics and crack propagation Adhesion measurement of thin films and coatings

One-stop, cutting-edge guide to flip chip technologies. Now you can turn to a single, all-encompassing reference for a practical understanding of the fast-developing field that's taking the electronics industry by storm. Low-Cost Flip Chip Technologies, by John H. Lau, brings you up to speed on the economic, design, materials, process, equipment, quality, manufacturing, and reliability issues related to low cost flip chip technologies. This eye-opening overview tells you what you need to know about applying flip chip technologies to direct chip attach(DCA), flip chip on board (FCOB), wafer level chip scale package (WLCSP), and plastic ball grid array (PBGA) package assemblies. You'll discover flip chip problem-solving methods, and learn how to choose a cost-effective design and reliable, high-yield manufacturing process for your interconnect systems as you explore... *IC trends and packaging technology updates *Over 12 different wafer-bumping methods...more than 100 lead-free solder alloys *Sequential build up PCB with microvias and via-in-pad *How to select underfill materials *And much, much more!

For more than 40 years, Computerworld has been the leading source of technology news and information for IT influencers worldwide. Computerworld's award-winning Web site (Computerworld.com), twice-monthly publication, focused conference series and custom research form the hub of the world's

largest global IT media network.

A follow-on to Micro- and Nanotechnology for Space Systems, this second monograph in the series uses the more universal term microengineering to define the discipline and processes that lead to the development of an integrated and intelligent microinstrument. Microengineering Technology for Space Systems addresses specific issues concerning areas for ASIM application in current space systems, operation in the space environment, ultra-high-density packaging and nonsilicon materials-processing tools, and the feasibility of the nanosatellite concept.

A comprehensive guide to TSV and other enabling technologies for 3D integration Written by an expert with more than 30 years of experience in the electronics industry, Through-Silicon Vias for 3D Integration provides cutting-edge information on TSV, wafer thinning, thin-wafer handling, microbumping and assembly, and thermal management technologies. Applications to highperformance, high-density, low-power-consumption, wide-bandwidth, and small-form-factor electronic products are discussed. This book offers a timely summary of progress in all aspects of this fascinating field for professionals active in 3D integration research and development, those who wish to master 3D integration problem-solving methods, and anyone in need of a low-power, wide-

bandwidth design and high-yield manufacturing process for interconnect systems. Coverage includes: Nanotechnology and 3D integration for the semiconductor industry TSV etching, dielectric-, barrier-, and seed-layer deposition, Cu plating, CMP, and Cu revealing TSVs: mechanical, thermal, and electrical behaviors Thin-wafer strength measurement Wafer thinning and thin-wafer handling Microbumping, assembly, and reliability Microbump electromigration Transient liquid-phase bonding: C2C, C2W, and W2W 2.5D IC integration with interposers 3D IC integration with interposers Thermal management of 3D IC integration 3D IC packaging

Today's electronics industry requires new design automation methodologies that allow designers to incorporate high performance integrated circuits into smaller packaging. The aim of this book is to present current and future techniques and algorithms of high performance multichip modules (MCMs) and other packaging methodologies. Innovative technical papers in this book cover design optimization and physical partitioning; global routing/multi-layer assignment; timing-driven interconnection design (timing models, clock and power design); crosstalk, reflection, and simultaneous switching noise minimization; yield optimization; defect area minimization; low-power physical layout; and design methodologies. Two tutorial reviews review some of the most significant

algorithms previously developed for the placement/partitioning, and signal integrity issues, respectively. The remaining articles review the trend of prime design automation algorithms to solve the above eight problems which arise in MCMs and other packages.

Clear your bookcase of references containing bits and pieces of useful information and replace them with this thorough, single-volume guide to thermal analysis. Air Cooling Technology for Electronic Equipment is a helpful, practical resource that answers questions frequently asked by thermal and packaging engineers grappling with today's demand for increased thermal control in electronics. Superbly organized for quick reference, the book dedicates each chapter to answering fundamental questions, such as: What is the optimal spacing between the printed circuit boards? What is a good estimate of the heat transfer coefficient and the associate pressure drop for forced convection over package arrays? How are heat transfer and fluid flow characteristics in the entrance region different from those in the fully developed region? What is the effect of substrate conduction on convection cooling? The chapters, written by engineers and engineering educators who are experts in electronic cooling, are packed with details and present the latest developments in air cooling techniques and thermal design guidelines. They provide problem-solving analyses that are

jargon-free, straightforward, and easy to understand. Air Cooling Technology for Electronic Equipment is a handy source of technical information for anyone who wants to get the most out of air cooling.

This handbook provides a comprehensive treatment of area-array interconnections for both chips and microelectronic packages in terms of optimizing densification, functionality and reliability. It provides comparisons with alternative and competing technologies, clearly defining cost versus benefit tradeoffs and strategies. Process details are defined in the order of their typical manufacturing sequence, indicating tooling requirements and potential yield detractors. In addition, the handbook has individual chapters devoted to supporting disciplines that play a key role in satisfying the requirements of microelectronic package applications: efficient thermal-dissipation techniques, metallurgical and mechanical characteristics of interconnections and electrical design strategies. Area-array technology at both die and chip carrier levels offers the best opportunity of satisfying the demanding performance requirements that users at all levels of the product spectrum have come to expect. This handbook fully describes the `how and why' of the inherent elements of area-array technology that give rise to enhanced electrical and thermal dissipation capabilities, and densification to accommodate demanding design requirements,

while at the same time accommodating size and cost reductions to enhance comfort and portability. This handbook is the only book that provides a complete and integrated treatment which includes all the aspects of area-array microelectronics. Each chapter is self contained, written in a clear, concise, easy-to-understand manner. It sets forth fundamentals followed by the application of those principles making prior knowledge of the subject material unnecessary in order to utilize this reference. The handbook will serve as an excellent text or companion reference for a variety of electronic packaging courses or workshops. FEATURES: describes all the key elements of microelectronic packaging technology; organized into three categories: die, chip carrier, and support technologies; presents information in a clear and concise manner; can be utilized as a textbook or companion reference for a range of microelectronic packaging courses; each chapter is self-contained; provides guidelines and strategies for making microelectronic packaging choices. ABOUT THE EDITORS: Considered `pioneers' in the field of microelectronics packaging, Karl Puttlitz and Paul Totta represent 80 years of experience in all aspects of the technology. They were key forces in the definition and implementation of flip-chip technology from its very inception at IBM and through its evolution during the past four decades. As major contributors in the development and manufacture of various microelectronics chip-

carrier packages, the authors are frequently invited to speak at universities, international conferences and workshops.

Far from being the passive containers for semiconductor devices of the past, the packages in today's high performance computers pose numerous challenges in interconnecting, powering, cooling and protecting devices. While semiconductor circuit performance measured in picoseconds continues to improve, computer performance is expected to be in nanoseconds for the rest of this century -a factor of 1000 difference between on-chip and off-chip performance which is attributable to losses associated with the package. Thus the package, which interconnects all the chips to form a particular function such as a central processor, is likely to set the limits on how far computers can evolve. Multichip packaging, which can relax these limits and also improve the reliability and cost at the systems level, is expected to be the basis of all advanced computers in the future. In addition, since this technology allows chips to be spaced more closely, in less space and with less weight, it has the added advantage of being useful in portable consumer electronics as well as in medical, aerospace, automotive and telecommunications products. The multichip technologies with which these applications can be addressed are many. They range from ceramics to polymer-metal thin films to printed wiring boards for interconnections; flip chip, TAB or

wire bond for chip-to-substrate connections; and air or water cooling for the removal of heat.

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Handbook of tape automated bonding (TAB) is a one-stop guide to the state of the art of TAB technology - including TAB tape, bump, inner lead bonding, encapsulation, testing, burn-in, outer lead bonding, inspection, rework, thermal management and reliability. For professionals active in TAB research and development, those who wish to master TAB problem solving methods, and those who must choose a high-performance and cost-effective packaging technique for their interconnect systems, here's a timely summary of progress in all aspects of this fascinating field.

An engineer's guidebook demonstrating non-toxic electronics manufacturing processes

Lists citations with abstracts for aerospace related reports obtained from world wide sources and announces documents that have recently been entered into the NASA Scientific and Technical Information Database.

Unfriendly to conventional electronic devices, circuits, and systems, extreme environments represent a serious challenge to designers and mission architects. The first truly comprehensive guide to this specialized field, Extreme Environment Electronics explains the essential aspects of designing and using devices, circuits, and electronic systems intended to operate in extreme environments, including across wide temperature ranges and in radiation-

intense scenarios such as space. The Definitive Guide to Extreme Environment Electronics Featuring contributions by some of the world's foremost experts in extreme environment electronics, the book provides in-depth information on a wide array of topics. It begins by describing the extreme conditions and then delves into a description of suitable semiconductor technologies and the modeling of devices within those technologies. It also discusses reliability issues and failure mechanisms that readers need to be aware of, as well as best practices for the design of these electronics. Continuing beyond just the "paper design" of building blocks, the book rounds out coverage of the design realization process with verification techniques and chapters on electronic packaging for extreme environments. The final set of chapters describes actual chip-level designs for applications in energy and space exploration. Requiring only a basic background in electronics, the book combines theoretical and practical aspects in each self-contained chapter. Appendices supply additional background material. With its broad coverage and depth, and the expertise of the contributing authors, this is an invaluable reference for engineers, scientists, and technical managers, as well as researchers and graduate students. A hands-on resource, it explores what is required to successfully operate electronics in the most demanding conditions.

Issues for 1973- cover the entire IEEE technical literature.

Driven by the fast-growing market for personal electronic devices, integrated circuit complexity has increased as feature sizes shrink. The resulting integrated circuit devices are prone to more frequent failures, which must be found, identified, and fixed. This unique reference uses graphic illustrations to clearly identify all major failure mode types, allowing engineers to spot failures before they occur.

Each May, the Continuing Education Division of the T.J.Watson School of Engineering, Applied Science and Technology at the State University of New York at Binghamton sponsors an Annual Symposium in Electronics Packaging in cooperation with local professional societies (IEEE, ASME, SME, IEPS) and UnlPEG (the University-Industry Partnership for Economic Growth.) Each volume of this Electronics Packaging Forum series is based on the the preceding Symposium, with Volume Two based on the 1990 presentations. The Preface to Volume One included a brief definition of the broad scope of the electronics packaging field with some comments on why it has recently assumed such a more prominent priority for research and development. Those remarks will not be repeated here; at this point it is assumed that the reader is a professional in the packaging field, or possibly a student of one of the many academic disciplines which contribute to it. It is worthwhile repeating the series objectives, however, so the reader will be clear as to what might be expected by way of content and level of each chapter.

A world list of books in the English language.

This book is a one-stop guide to the state of the art of COB technology. For professionals active in COB and MCM research and development, those who wish to master COB and MCM problem-solving methods, and those who must choose a cost-effective design and high-yield manufacturing process for their interconnect systems, here is a timely summary of progress in al aspects of this fascinating field. It meets the reference needs of design, material, process, equipment, manufacturing, quality, reliability, packaging, and system engineers, and technical managers working in electronic packaging and interconnection.